Integrating electrical wafer sorting and complete-line process control data for optimizing process and equipment performance

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1 Context and motivations

In semiconductor manufacturing, Statistical Process Control (SPC) and Fault Detection and Classification (FDC) are essential for ensuring product compliance with Electrical Wafer Sort (EWS) specifications at the end of the line. Modern wafer fabrication involves hundreds of process steps (i.e., operations), many of which can be performed by multiple tools. To prevent yield losses, operations are statistically monitored and controlled via process control frameworks. As illustrated in Figure 1, FDC collect high-frequency equipment traces at the wafer level to detect abnormal tool behavior and support root cause analysis. SPC systems monitor process stability using inline metrology measurements to detect defects. EWS tests evaluate chips on the wafer through hundreds to over a thousand conformance checks to ensure compliance with customer specifications.

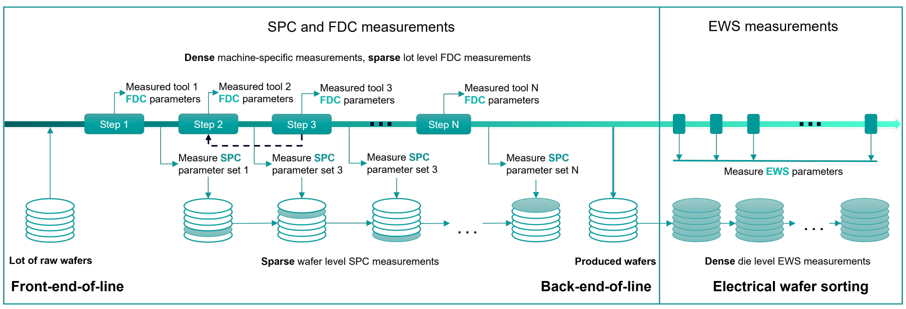

FIG. 1: Modeling full production line from FEOL to BEOL via SPC, FDC, and EWS data.

In practice, yield detractors are commonly identified through characteristic patterns known as *anomaly signatures* (e.g., rings, scratches, clusters). Early methods for wafer map pattern recognition are mainly manual or rule-based. Engineers visually inspect wafer maps and apply heuristics to identify patterns. As data volumes grew, engineers turned to machine learning-based algorithms to improve wafer map anomaly classification [1, 2]. However, in real-world manufacturing environments, novel and previously unseen anomaly signatures continue to emerge within the vast amount of EWS maps generated daily. Consequently, it is infeasible to define a finite and exhaustive set of such signatures, as this would fail to capture the dynamic and evolving nature of actual manufacturing scenarios.

To address this limitation, we propose reframing the problem as a regression task aimed at uncovering interdependencies between EWS maps and SPC data. The objective is to identify, in a first stage, the operations and associated equipment most likely responsible for electrical drifts. This enables a more targeted root-cause analysis and facilitates a focused optimization of the associated process parameters via FDC data.

2 Solution approaches, validation, and industrial implications

We propose a comprehensive modeling framework that spans the full production flow, from the front-end-of-line to the back-end-of-line, SPC data with EWS outcomes. A regression-based modeling approach has been employed to uncover interdependencies between SPC and EWS data at the lot level per product. Three modeling approaches are introduced: **(i) Single-target approach**, which models each EWS target independently, allowing for fine-grained prediction of individual EWS targets; **(ii) Multi-target approach**, which predicts related EWS targets jointly, enabling the capture of intra-family dependencies; **(iii) Canonical approach**, which treats all EWS targets simultaneously, thereby capturing shared variance structures and monotonic relationships across the full set of targets.

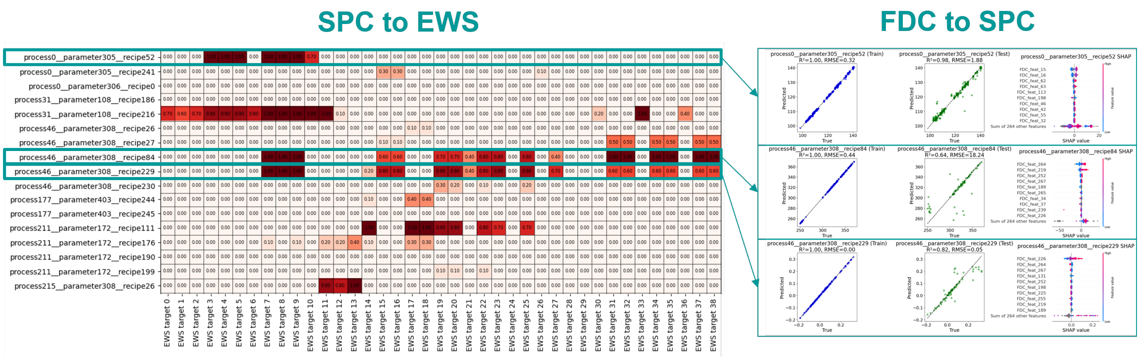

FIG. 2: Workflow from EWS to critical operations (SPC) to process recipes (FDC)

To evaluate the industrial relevance of the proposed solution approaches, computational experiments were carried out based on real-life data. The results demonstrate the ability of the models to identify critical operations and equipment contributing to electrical drifts. As an extension, FDC data is integrated to identify the process parameters that require adjustment. This integration aims to guide the optimization of manufacturing conditions, thereby enhancing the performance of the manufacturing system of interest.

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